REMARKS

The Examiner is thanked for indicating the allowability of claims 7, 8, and 15. Accordingly, these claims are now submitted hereto in independent form in new claims 16, 17, and 18.

New claim 16 is directed towards a method for erasing non-volatile memory cells and incorporates features of claim 7, which was considered allowable subject matter based on Harari et al., U.S. Patent Number 5,418,752, in view of Horiguchi et al., U.S. Patent Number 5,265,055, and Horiguchi et al., U.S. Patent Number 5,262,993. New claim 17 depends upon claim 16 and incorporates features of claim 8, which was considered allowable subject matter based on Harari in view of Horiguchi '055 and Horiguchi '993. Thus, new claims 16-17 are in condition for allowance.

New claim 18 is directed toward an integrated non-volatile memory device of the programmable and electrically erasable type and incorporates features of claim 15, which was considered allowable subject matter based on Horiguchi '055 and Horiguchi '993. Thus, new claim 18 is in condition for allowance.

Submitted herewith are amended claims 4, 14, and 15. Submitted herewith are new claims 16-18. All other claims remain unamended. The first paragraph of the specifications has now been amended to update the co-pending application with an application serial number. No new matter is presented.

In the Office Action mailed February 8, 2005 claims 4 and 14 were objected to for failing to meet proper formalities. Claims 4 and 14 have now been amended to meet the specified requirements.

Claim 15 is amended to fix minor grammatical errors.

Claim 1 and dependent claims 2-6 and 9-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Harari et al., U.S. Patent Number 5,418,752, in view of Horiguchi et al., U.S. Patent Number 5,265,055, and Horiguchi et al., U.S. Patent Number 5,262,993.

Claims 11-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Horiguchi '055, in view of Horiguchi '993.

Applicants respectfully disagree with the bases for the rejections and request reconsideration and further examination of the claims.

Claim Rejections 35 U.S.C. § 103

With respect to claim 1, the Examiner cites column 7, lines 6-8 as an example of how Harari checks the possible presence of a spurious current to indicate a fail state. However, the example cited is not a teaching or a suggestion of using a spurious current to detect a fail state but simply an acknowledgment that spurious current exists in a fail state and that it is undesirable. Harari does not teach or suggest a method for using the spurious current to detect a failed state.

Instead, Harari detects hard errors by their failure to program or erase properly (column 8 line 29-31). To detect failures, the controller compares the value stored into a desired cell with the value entered (column 10 line 40-48). If a match is made, the data is allowed to be stored; however, if a match is not made, the ECC (error correction code) registers an error. The process of continuous error detection and dynamic defect mapping continues from there. Thus, there is no teaching or suggestion that a defective cell is detected by the method suggested in claim 1. Claim 1 is directed towards a method for scanning the rows of an erased sector to check for the possible presence of a spurious current indicating a fail state.

In addition, both Horiguchi patents relate to general structures for memory layouts, namely a memory matrix with additional blocks used for redundancy. These references should be considered reflecting the prior art knowledge as described in Harari, U.S. Patent Number 5,418,752. Accordingly, claim 1 and all other dependent claims thereto are in condition for allowance.

With respect to claim 11, the Examiner cites Horiguchi, U.S. Patent Number 5,262,055, as disclosing a memory device with a plurality of row decode blocks with at least one redundancy decode block within the decode circuitry. However, as evidenced by Figure 9 and other related figures, the redundancy decode block in Horiguchi '055 is not actually within the

decode circuitry. The redundancy decode block in Horiguchi '055 is separate and apart from the decode circuitry. In Figure 9 and all other related figures, the spare word line selection circuit 600 is different and not within the Y-decoders 400 or the X-decoders 300-301 (see for example column 8, lines 5-8 and column 18, lines 16-19).

On the other hand, claim 11 is directed toward an integrated non-volatile memory device with a plurality of decode blocks with at least one redundancy decode block within the decode circuitry. Accordingly, claim 11 and all other dependent claims are in condition for allowance.

Information Disclosure Statement

The listing of references in the specification, particularly in the first paragraph of the specifications, has already been included in the original Information Disclosure Statement filed on September 30, 2003. Thus, the applicants respectfully ask for consideration of reference with U.S. Application No. 10/675,805.

Drawing Objections

The drawings were objected to under 37 CFR 1.121(d) for failure to designate by a legend Figures 1-3 as "Prior Art". Replacement Sheets are provided that reflect this requirement and are presented herewith for approval.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

David V. Carlson
Registration No. 31,153

DVC:lcs

Enclosures:
Postcard
8 Replacement Sheets Drawings (Figs. 1-12)

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

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Amendments to the Drawings:

The attached sheets of drawings include changes to Figures 1-3. These sheets, which include Figures 1-12, replace the original sheets including Figures 1-12.

Attachment: Replacement Sheets